

**XEBEC**  
**432 LAKESIDE DRIVE**  
**SUNNYVALE, CALIFORNIA 94086**

**S-1401**  
**GENERAL PURPOSE DISK CONTROLLER**  
**FOR 8" AND 5½"**  
**FLOPPY DISK DRIVES**

**100052 REVISION C**  
**OWNER'S MANUAL**

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## CHAPTER 1

### INTRODUCTION

#### 1.1 GENERAL

The S-1401 Floppy Disk Controller, referred to as the FDC, can control the operation of up to four 8-inch or 5½-inch floppy disk drives that have interfaces that are compatible with the standard floppy interface. This means that the FDC can operate with a large class of 8-inch and 5½-inch disk drives.

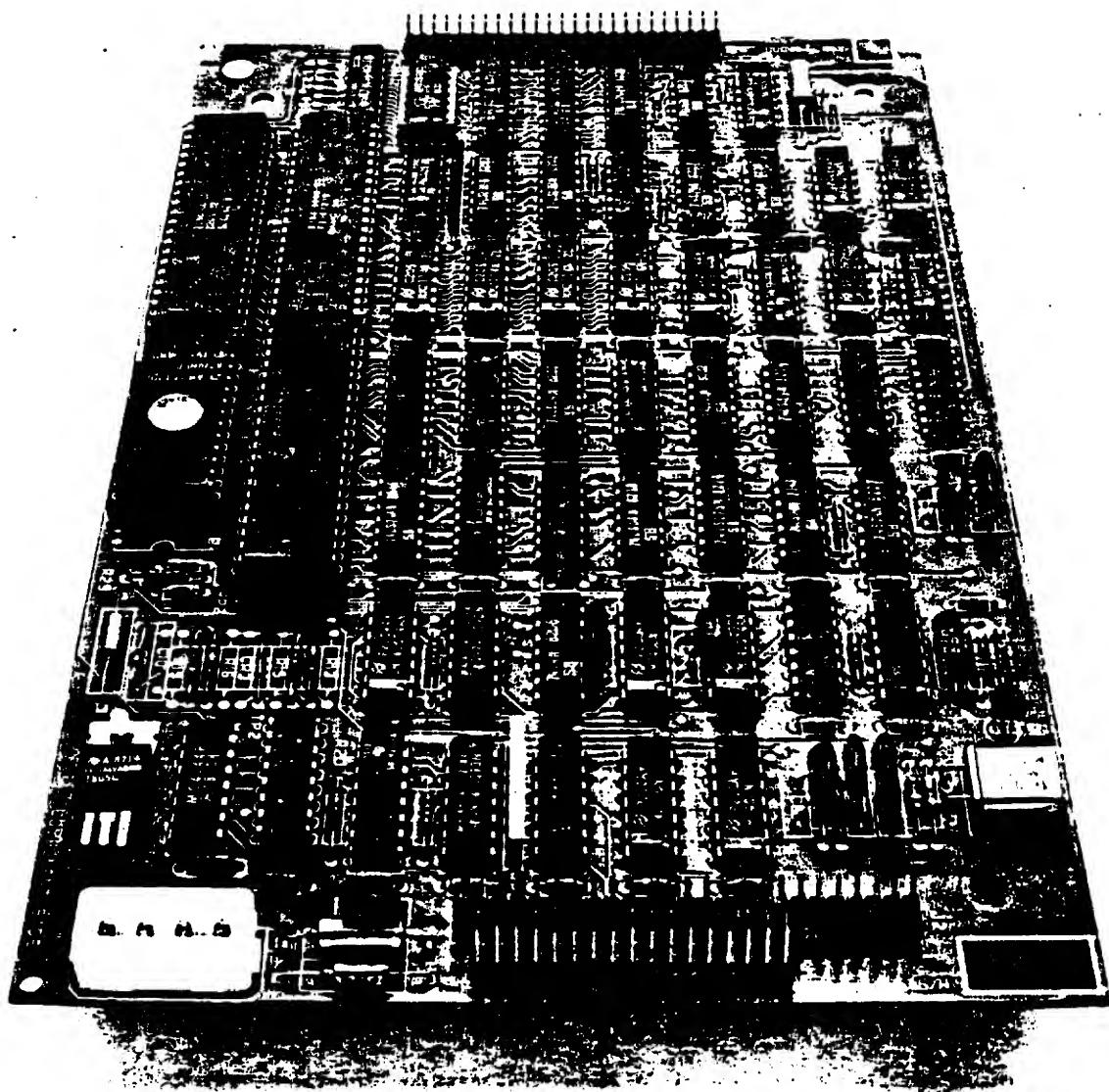
#### 1.2 DESCRIPTION

The FDC, shown in Figure 1-1, is packaged on a compact printed circuit board whose dimensions are 5-3/4 by 8 inches. Because the controller uses the Shugart Associates System Interface (SASI), it does not require special or complex design considerations in order to communicate with popular host buses. The following list highlights the operating and design features of the controller.

- Interlocked data transfer through the Shugart Associates System Interface (SASI).
- Microprocessor-based architecture (patent pending).
- Full-sector buffer.
- Automatic retries during disk access.
- Internal Diagnostics.
- Automatic burst error detection.
- Separate sector format for ID and data fields with individual CRC fields for both the ID and data fields.
- High level command set.

#### 1.3 FUNCTIONAL ORGANIZATION

The simplified block diagram in Figure 1-2 shows the functional organization of the Controller. Only the major areas are shown.



**FIGURE I-1 FLOPPY CONTROLLER**

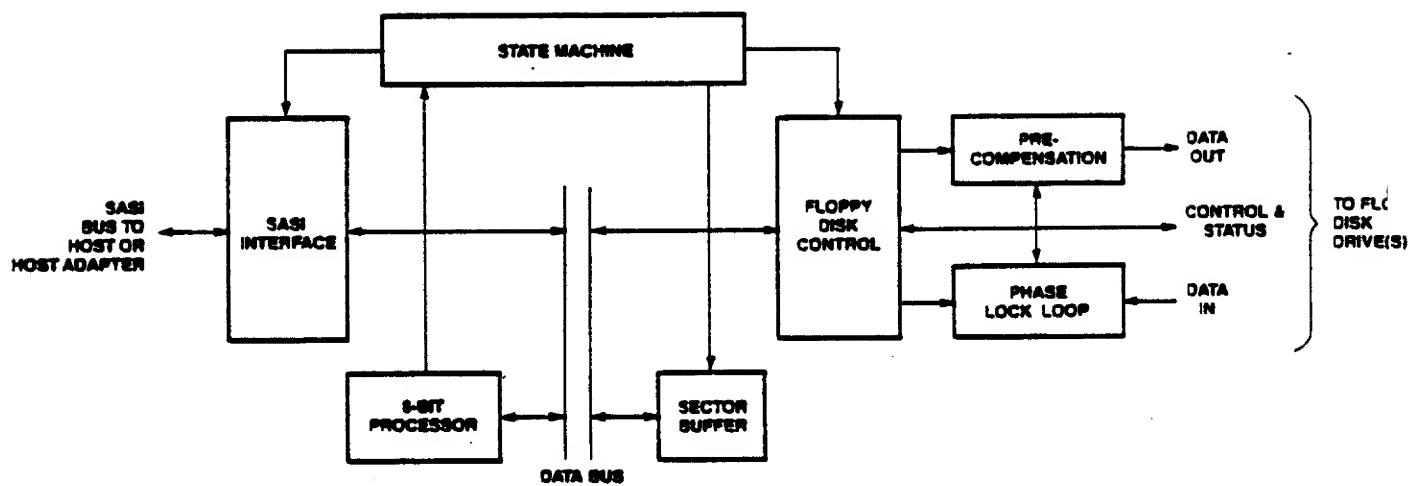


FIGURE 1-2 FLOPPY DISK CONTROLLER, FUNCTIONAL ORGANIZATION

**1.3.1 Host Interface**

The host interface connects the internal data bus to the host adapter; the state machine controls the movement of data and commands through the host interface.

**1.3.2 Processor**

The eight-bit processor is the intelligence of the controller; it monitors and controls the operation of the controller.

**1.3.3 State Machine**

The state machine controls and synchronizes the operation of the host adapter, and the FDC chip.

**1.3.4 Floppy Disk Controller**

The Floppy Disk Controller is an LSI chip that controls the interface between the controller and the floppy disk. These functions include seek, read and write.

**1.3.5 Phase Lock Loop**

The phase lock loop locks onto different data rates so that this single controller can accurately recover high density and low density data from both the faster 8" drive and the slower 5 $\frac{1}{4}$ " drive.

**1.3.6 Sector Buffer**

The sector buffer stages data transfers between the disk and the host to prevent data overruns.

**1.3.7 Pre-Compensation**

The write data pulses are shaped to provide optimum recovery waveforms.

## CHAPTER 2 SPECIFICATIONS

### 2.1 GENERAL

This chapter contains the overall specifications for the Controller. These specifications are meant to guide the user in placing the controller into operation. Some of the specifications indicate limits; the user must adhere to these in order to operate the controller successfully.

### 2.2 ELECTRICAL

Table 2-2 lists the electrical requirements of the controller.

**Table 2-1 Controller Electrical Requirements**

<u>Voltage</u>	<u>Range</u>	<u>Current</u>
+5.0 Vdc	4.75 to 5.25 Vdc	1.9 Amp. Max.
		1.4 Amp. Typ.
+12.0 Vdc	10.8 to 13.2 Vdc	20 mA. Max.
		10 mA. Typ.

**Note:** The maximum conducted power supply ripple must not exceed 0.10 volts rms.

### 2.3 PHYSICAL SPECIFICATIONS

Table 2-1 lists the specifications of the controller board and Figure 2-1 illustrates the dimensions of the board.

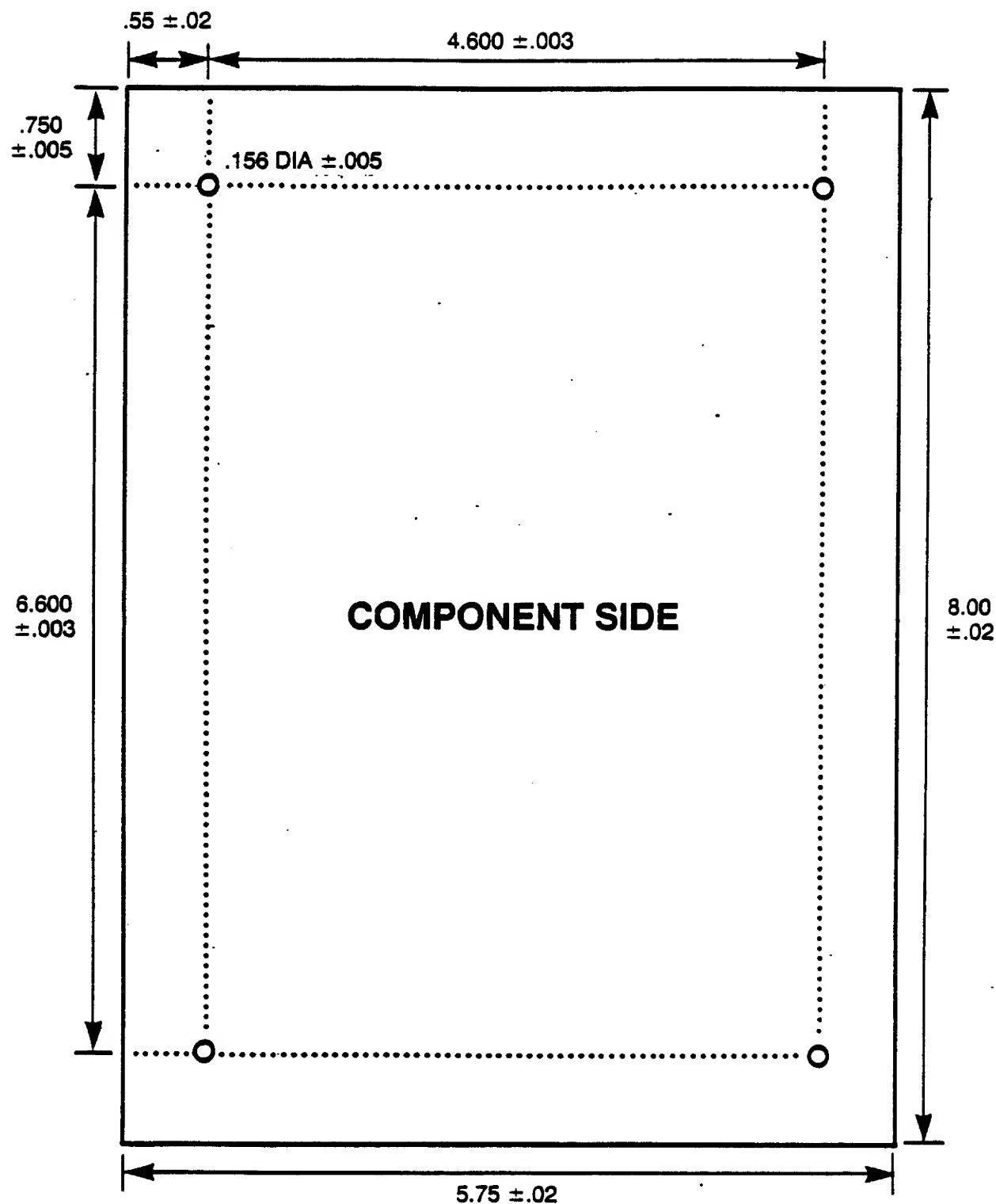


FIGURE 2-1 CONTROLLER BOARD DIMENSIONS

**TABLE 2-2 CONTROLLER BOARD SPECIFICATIONS**

<u>ITEM</u>	<u>MEASUREMENT</u>
Width (W)	5.75 inches
Length (L)	8.00 inches
Height (H)	0.60 inches
(Board thickness, components and lead protrusion)	
Weight	8.0 ounces

**2.4 ENVIRONMENTAL REQUIREMENTS**

The controller will operate under the environmental conditions listed in Table 2-3. The controller does not normally require fans in standard operating environments where airflow is not restricted.

**TABLE 2-3 ENVIRONMENTAL LIMITS**

<u>ITEM</u>	<u>MEASUREMENT</u>
Temperature	0 to 50 degrees Celsius
Relative Humidity	10 to 95 percent
Altitude	Sea level to 10,000 feet

**2.5 CONNECTORS**

Table 2-5 lists the Controller mating connectors.

**TABLE 2-4 CONTROLLER MATING CONNECTORS**

<u>DESIG-</u>	<u>FUNCTION</u>	<u>TYPE/SOURCE</u> <u>(OR EQUIVALENT)</u>
J1	Drive control signals (8 inch)	AMP 88373-1
J2	Drive control signals (5½ inch)	AMP 88373-3
P1	Power Supply	AMP 1-480424-0 (housing) AMP 350078-4 (pins)
P2	Host interface signals	AMP 86916-1

## 2.6 CONNECTOR PIN ASSIGNMENTS

Tables 2-5 through 2-7 list the pin assignments of the connectors on the controller board. The tables identify the signals on the pins. The signals in Table 2.6 are defined in Chapter 4, Theory of Operation.

**TABLE 2-5 CONNECTOR J1 AND J2  
FLOPPY DISK SIGNALS, PIN ASSIGNMENTS**

<u>SIGNAL PIN</u>	<u>J2 8" FLOPPY</u>	<u>J1 5½" FLOPPY</u>
2	Low Current	-
4	-	In use-
6	-	Drive Select 3-
8	-	Index-
10	Two Sided-	Drive Select 0-
12	Door Opened-	Drive Select 1-
14	Side Select-	Drive Select 2-
16	In Use-	Motor On-
18	Head Load-	Direction-
20	Index-	Step-
22	Ready-	Write Data-
24	-	Write Enable-
26	Drive Select 0-	Track 00-
28	Drive Select 1-	Write Protect-
30	Drive Select 2-	Read Data-
32	Drive Select 3-	Side Select-
34	Direction-	-
36	Step-	
38	Write Data-	
40	Write Enable-	
42	Track 00-	
44	Write Protect-	
46	Read Data-	
48	-	

**TABLE 2-6 CONNECTOR P2, HOST INTERFACE PIN ASSIGNMENTS**

<u>PIN NUMBER</u>	<u>SIGNAL NAME</u>
2	DATA0-
4	DATA1-
6	DATA2-
8	DATA3-
10	DATA4-
12	DATA5-
14	DATA6-
16	DATA7-
18	Spare
20	Spare
22	Spare
24	Spare
26	Spare
28	Spare
30	Spare
32	Spare
34	Spare
36	BUSY-
38	ACK-
40	RST-
42	MSG-
44	SEL-
46	C/D
48	REQ-
50	I/O

**TABLE 2-7 CONNECTOR P1, POWER SUPPLY, PIN ASSIGNMENTS**

<u>PIN NUMBER</u>	<u>VOLTAGE</u>
1	+12 Vdc
2	Ground return
3	Ground return
4	+5 Vdc

## CHAPTER 3

### BOARD SETUP

#### 3.1 GENERAL

This chapter contains the information for setting up and installing the controller before placing it in operation. These preparatory steps require the proper placement of jumpers, mounting the controller in its operating environment, and properly connecting the cables. In addition, the user has the option of using more than one controller with the host adapter in his system. Instructions for connecting multiple controllers appear later in the chapter.

#### 3.2 MOUNTING CONTROLLER

The controller board has four mounting holes. It can be mounted anywhere within the drive enclosure so long as it receives airflow.

#### 3.3 CONNECTING CABLES

Before the controller can be placed in operation, the cables to the drive and host must be connected. These cables are listed below:

J1 or J2 Drive Cable: maximum 20 feet (controller to last drive)

P1 Power Cable

P2 Host Interface Cable: maximum 15 feet

Figure 3-3 shows the connector locations.

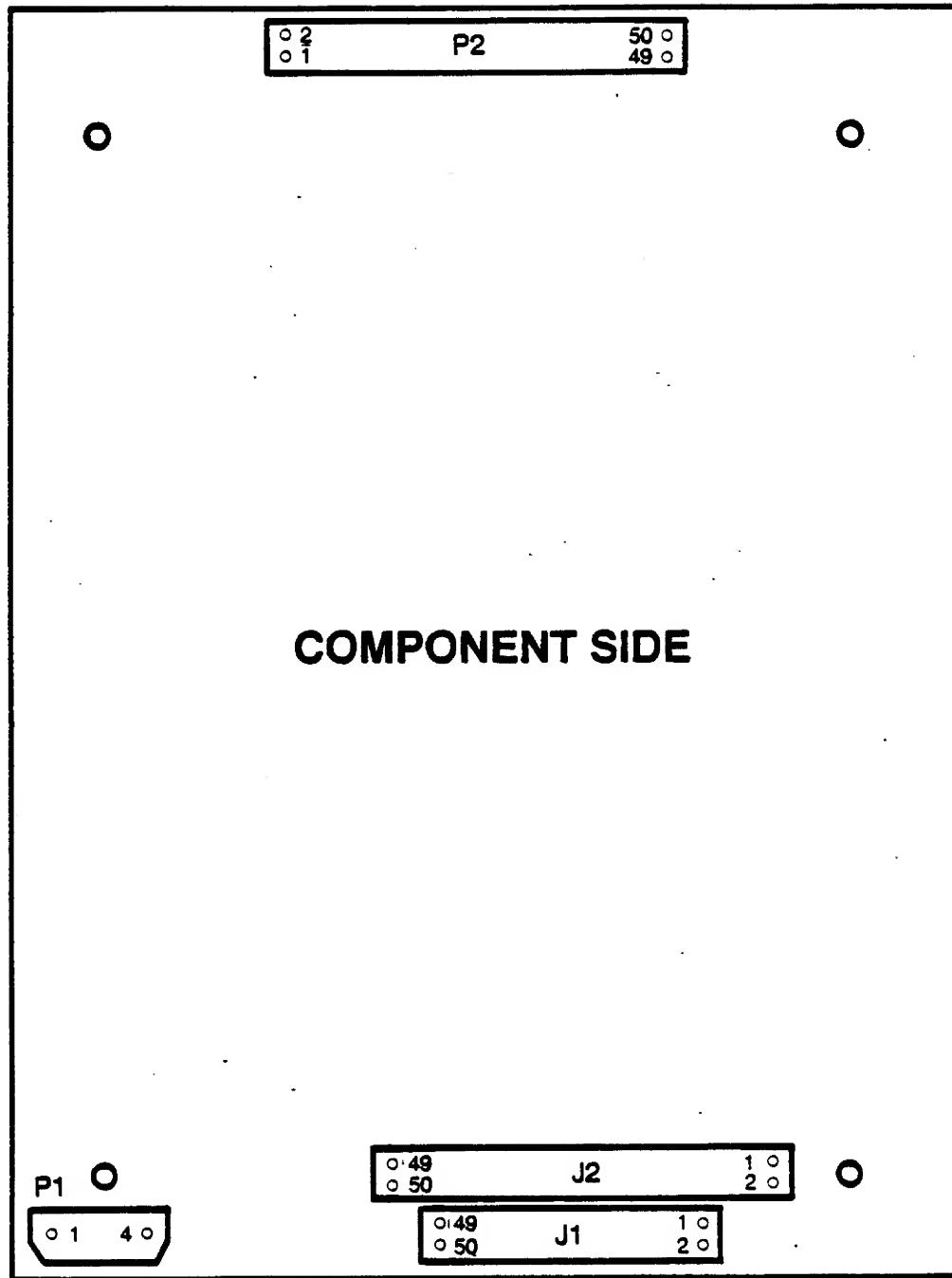


FIGURE 3-1 CONNECTOR LOCATIONS

### 3.4 MULTIPLE CONTROLLERS

A separate controller is required for each additional set of four drives. Figure 3-2 shows two operating setups: (A) using one controller and (B) using two controllers. Notice the terminator (resistor pack) in both drawings. The terminator is in a socket near Pin 1 on connector P2; when multiple controllers are used, the terminator must be installed only in the last board on the daisy chain.

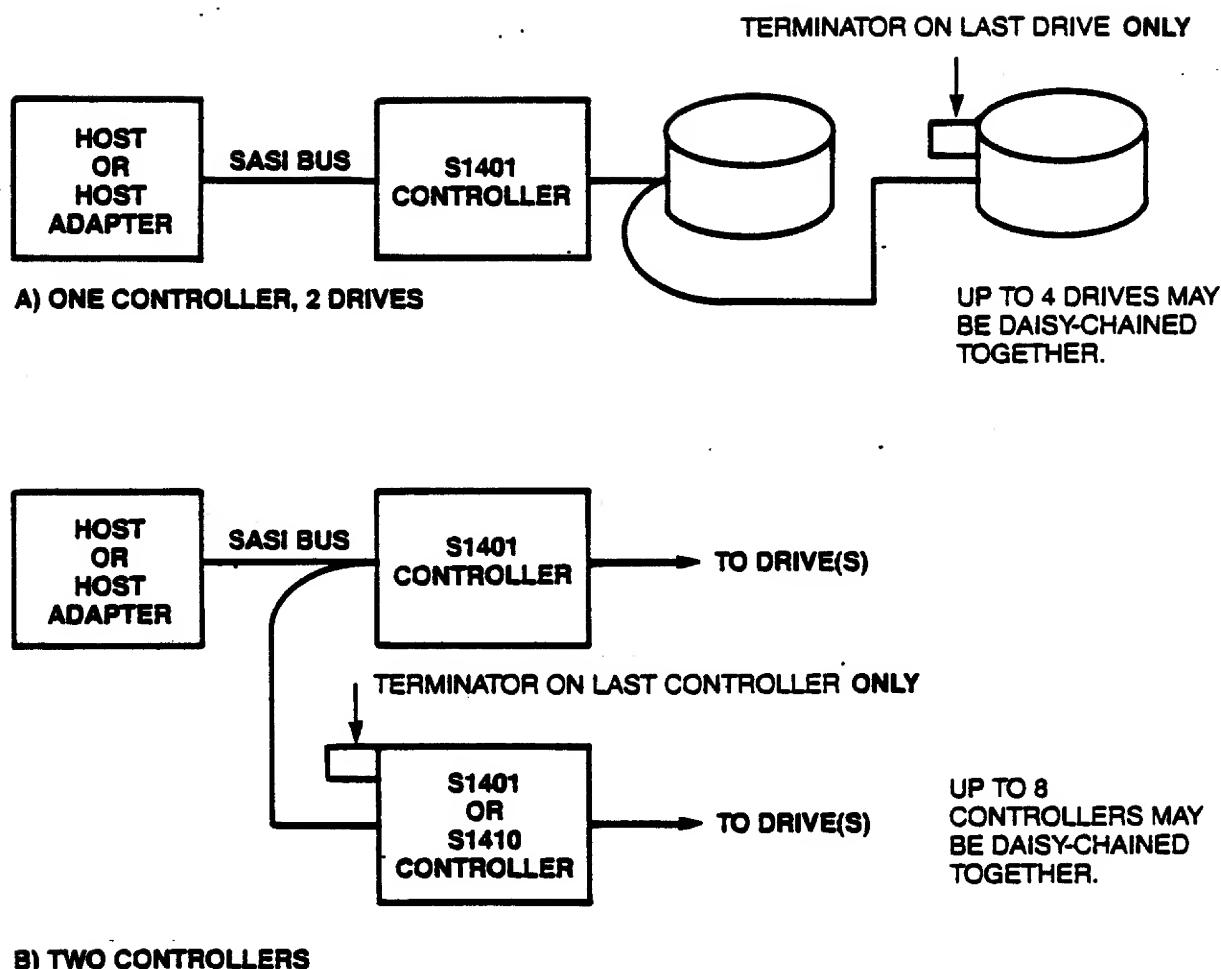
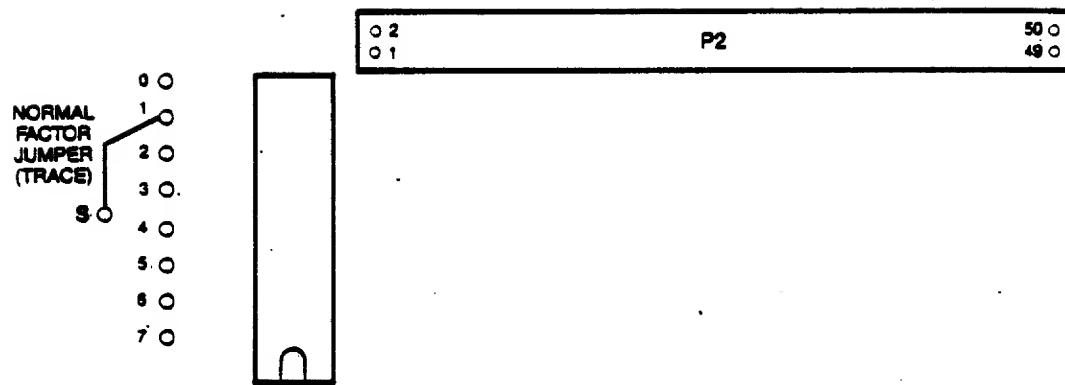


FIGURE 3-2 OPERATING SETUPS

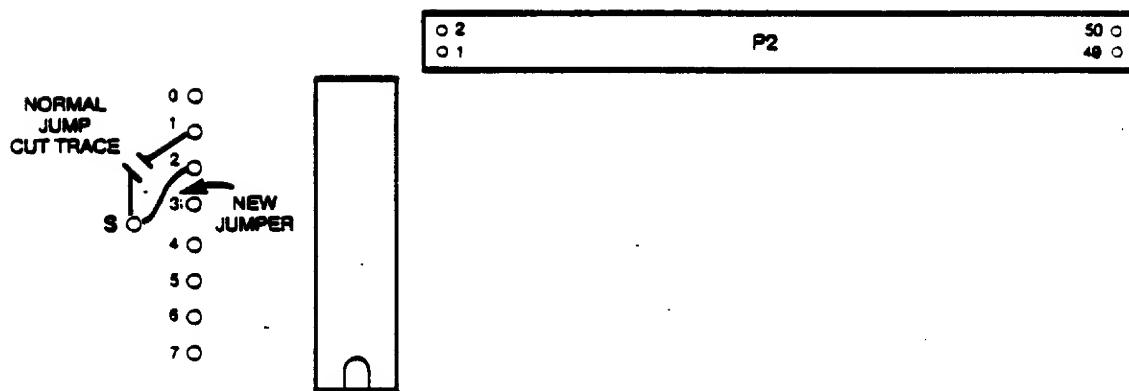
### 3.5 ADDRESS JUMPER GROUP

The Controller supports one of eight unique device addresses. When more than one controller is used in a system, the address jumper on the controller must be changed. Figure 3-3 shows the address jumper group located near the mounting hole by connector P2, pin 1; it also shows that terminal (pad) 1 is connected to terminal S. This is the factory-installed jumper, and it sets the controller's address to 1.

In order to change this address, the factory-installed jumper (trace) must be cut. Then, a new jumper must be connected between terminal S and the selected address terminal. Figure 3-3 shows that the factory-installed jumper has been cut, and a new jumper has been installed between terminal S and address terminal 2. The address of the controller is now 2.



**NORMAL (FACTORY-INSTALLED) ADDRESS JUMPER**



**CHANGED ADDRESS JUMPER (CONTROLLER 2)**

**FIGURE 3-3 ADDRESS JUMPER**

## CHAPTER 4

### THEORY OF OPERATION

#### 4.1 GENERAL

This chapter discusses the theory of operation of the FDC and lays down the guidelines that will enable the user to use the controller successfully in any number of applications.

##### 4.1.1 Conventions

Signals or lines can be active in either a high or low state. The terms signal, signal lines, and lines mean the same thing. A low state is equivalent to a voltage level of 0.8 volts or less, and a high state is equivalent to a voltage level of 2.4 volts or more.

##### 4.1.2 Names and Abbreviations

A dash (-), or the lack of one, indicates the active state of a signal. The active state of a signal is that state which is required for a given operation. When a dash is appended to end of a signal name, the signal is active when it is low. When no dash appears at the end of a signal name, the signal is active when it is high. Some signal lines have two so-called active (or significant) states. When the level on the line is high, a particular operation takes place. When the level on the line is low, a different operation takes place. The following examples show the use of these conventions.

**BUSY-** The signal BUSY- is active when it is at a low level because it has the dash appended.

**BUSY** The signal BUSY is active at a high level because it does not have the dash appended.

**C/D** The line C/D (command/data) has a dual purpose; the standard slash (/) indicates duality. It is not apparent what the active states are. The user must look up the definition in the appropriate table.

Other designations used to define signal lines are listed below.

Drv	Driver
Rcvr	Receiver
OC	Open collector
Tri-State	Line has three states: high, low, high impedance
220/330	Line termination (on the controller): 220 Ohms to source voltage/330 Ohms to ground.

#### 4.1.3 Signal Definitions

The following tables list and define the signals that appear on the lines between the host adapter and the controller.

**TABLE 4-1 HOST BUS STATUS SIGNALS**

<u>NAME</u>	<u>DRV/RCVR</u>	<u>DEFINITION</u>
I/O	Drv OC	Input/Output: The controller driving REQ- drives this line. A low level on this line indicates that the controller is driving the data on the host bus. A high level on this line indicates that the controller is expecting someone else to drive the data on the SASI bus. This signal is qualified by signal REQ-.

C/D	Drv OC	Command/Data: The controller driving REQ- drives this signal line to indicate whether the information on the data bus consists of command or data bytes. A low means command bytes; a high means data bytes. This signal is qualified by signal REQ-.
BUSY-	Drv OC	Busy: The controller generates this active low signal in response to the SEL-signal and the address bit (DB0- to DB7-) from the host adapter. The busy signal informs the host adapter the controller is ready to conduct transactions on the host bus.
MSG-	Drv OC	Message: The controller driving REQ- asserts this active low signal to indicate that the current command has been completed. When MSG- is active, the I/O signal line is always low so that the controller can drive the bus data lines. This signal is qualified by signal REQ-.

**TABLE 4-2 SUMMARY OF HOST BUS STATUS SIGNALS**

<u>I/O</u>	<u>C/D</u>	<u>MSG-</u>	<u>DEFINITION</u>
High	Low	High	The controller receives a command from the host adapter.
High	High	High	The controller receives data from another source on the SASI bus.
Low	High	High	The controller sends data over the SASI bus.
Low	Low	High	The controller sends error status byte to the host adapter.
Low	Low	Low	The controller informs the host adapter that it has completed the current command.

**TABLE 4-3 CONTROLLER-HOST ADAPTER HANDSHAKING**

<u>NAME</u>	<u>DRV/RCVR</u>	<u>DEFINITION</u>
REQ-	Drv OC	<p><b>Request:</b> The controller sends this active low signal to the host adapter to initiate the controller-host handshaking sequence. This signal qualifies signals I/O, C/D and MSG-. When executing a copy command, the controller looks at this signal to know when the other controller expects a data transfer.</p>
ACK-	Rcvr, 220/330	<p><b>Acknowledge:</b> The host adapter generates this active low signal in response to the REQ- signal from the controller when the host is ready to receive or transmit data. In order to complete the handshake, the host adapter must send an acknowledge (ACK-) in response to each request (REQ-) from the controller. When executing a copy command, the controller will assert this in response to another controller's REQ- to acknowledge the data transfer.</p>

TABLE 4-4 HOST BUS CONTROL SIGNALS

<u>NAME</u>	<u>DRV/RCVR</u>	<u>DEFINITION</u>				
RST-	Rcvr, 220/330	<p>Reset: The host adapter sends this negative edge triggered signal to the controller to force the controller to the idle state. After RST- has become active, any controller status is cleared. RST- also causes the deactivation of all signals to the drives. The time requirements for the RST- signal are as follows:</p> <table> <thead> <tr> <th><u>Minimum</u></th><th><u>Maximum</u></th></tr> </thead> <tbody> <tr> <td>100 nsec.</td><td>None</td></tr> </tbody> </table> <p>You must allow 50 microseconds between asserting RST- and asserting SEL-. The automatic reset when power is first turned on lasts 500 milliseconds.</p>	<u>Minimum</u>	<u>Maximum</u>	100 nsec.	None
<u>Minimum</u>	<u>Maximum</u>					
100 nsec.	None					
SEL-	Rcvr, 220/330	Select: The host adapter sends this active low signal to the controller to initiate a command transaction. Along with SEL-, the host adapter must also send an address bit to select the controller (DB0- for controller 0). The controller must not be busy. The host adapter must deactivate SEL- before the end of the current command, or before the SASI data bus is used if another controller is on the SASI bus.				

**TABLE 4-5 HOST BUS DATA SIGNAL**

<u>NAME</u>	<u>DRV/RCVR</u>	<u>DEFINITION</u>
DB7- to DB0-	Tri-State, 220/330	<p>These are the eight data bits (lines) of the host bus (DB0- = LSB). Each line is also used as address bits to select a controller in systems using multiple controllers (see Chapter 3). The normal connection (hardwired on the board) is to DB1- which is the address of controller 1. Any other connection requires cutting the existing trace on the board and adding a jumper.</p>

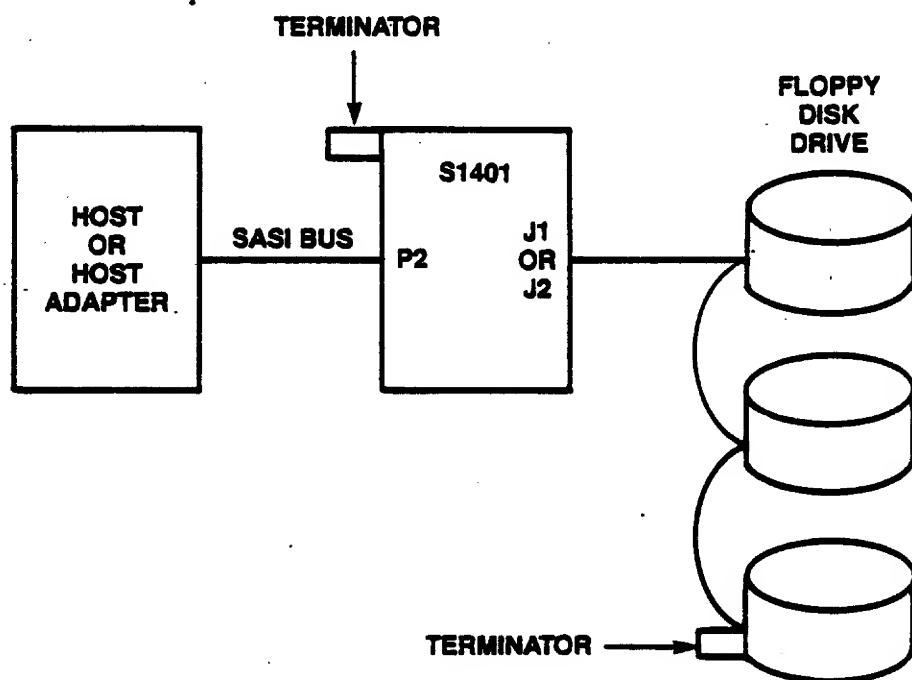
The following list shows the bit assignments.

DB0-	Controller 0
DB1-	Controller 1
DB2-	Controller 2
DB3-	Controller 3
DB4-	Controller 4
DB5-	Controller 5
DB6-	Controller 6
DB7-	Controller 7

#### 4.2 BASIC OPERATING CONFIGURATION

The basic operating configuration consists of a host adapter, Floppy Disk Controller, and a Floppy disk drive with an interface that is compatible with the standard floppy disk drive. Figure 4-1 shows the basic setup.

The host can be one of a number of computer systems; the host adapter is an interface between the host's bus and the controller.



**FIGURE 4-1 BASIC OPERATING CONFIGURATION**

Note up to 4 drives may be connected and the terminator must be on the last drive. Three are shown above.

J1 should be used for 5 $\frac{1}{4}$ " drives.

J2 should be used for 8" drives.

**Note: You cannot connect both 8" and 5 1/4" drives at the same time.**

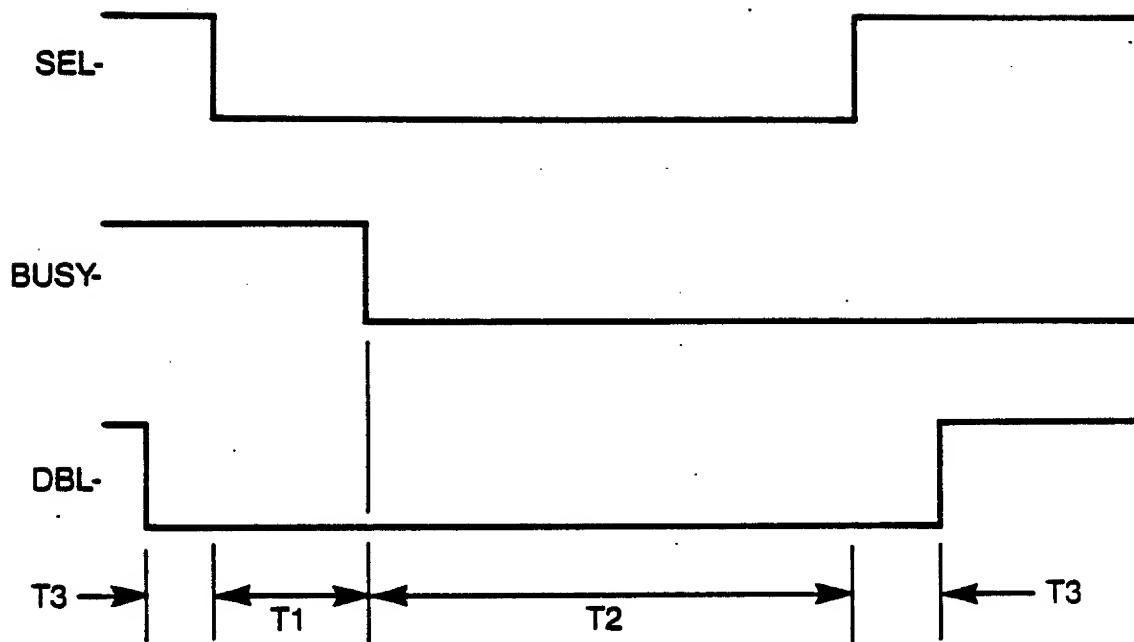
#### 4.3 DETAILED DESCRIPTION

The following paragraphs describe the interaction between the controller and the host adapter.

##### 4.3.1 Controller Selection

Before the host adapter can begin a transaction, it must select the controller. The host adapter selects the controller by activating the SEL- control signal and the address bit of the controller. Any bit, DB0- through DB7-, can be the address bit in a system with multiple controllers (all controllers leave the factory with DB1- connected to the controller's address logic). For this discussion, the controller's address is 1.

The timing diagram in Figure 4-2 shows the basic timing requirements. Upon receiving both the SEL- signal and DB1-, the controller activates the BUSY- signal. As shown in the timing diagram, both SEL- and DB1- must be active (low) before the controller can activate the BUSY- signal. During the selection process, the host has control of the data bus as signified by the deactivation of the I/O line. Selection is complete when BUSY- becomes active. The Controller then enters the command mode.



**FIGURE 4-2 CONTROLLER SELECT TIMING**

T1 50 nanoseconds (typical)

T2 no time limit. However, if more than one controller is on the SASI Bus, SEL- must be cleared (brought inactive, high) before the data bus is used. If only one controller, it's best to clear SEL- sometime before the controller finishes its command.

T3 100 nanoseconds min. (2 places)

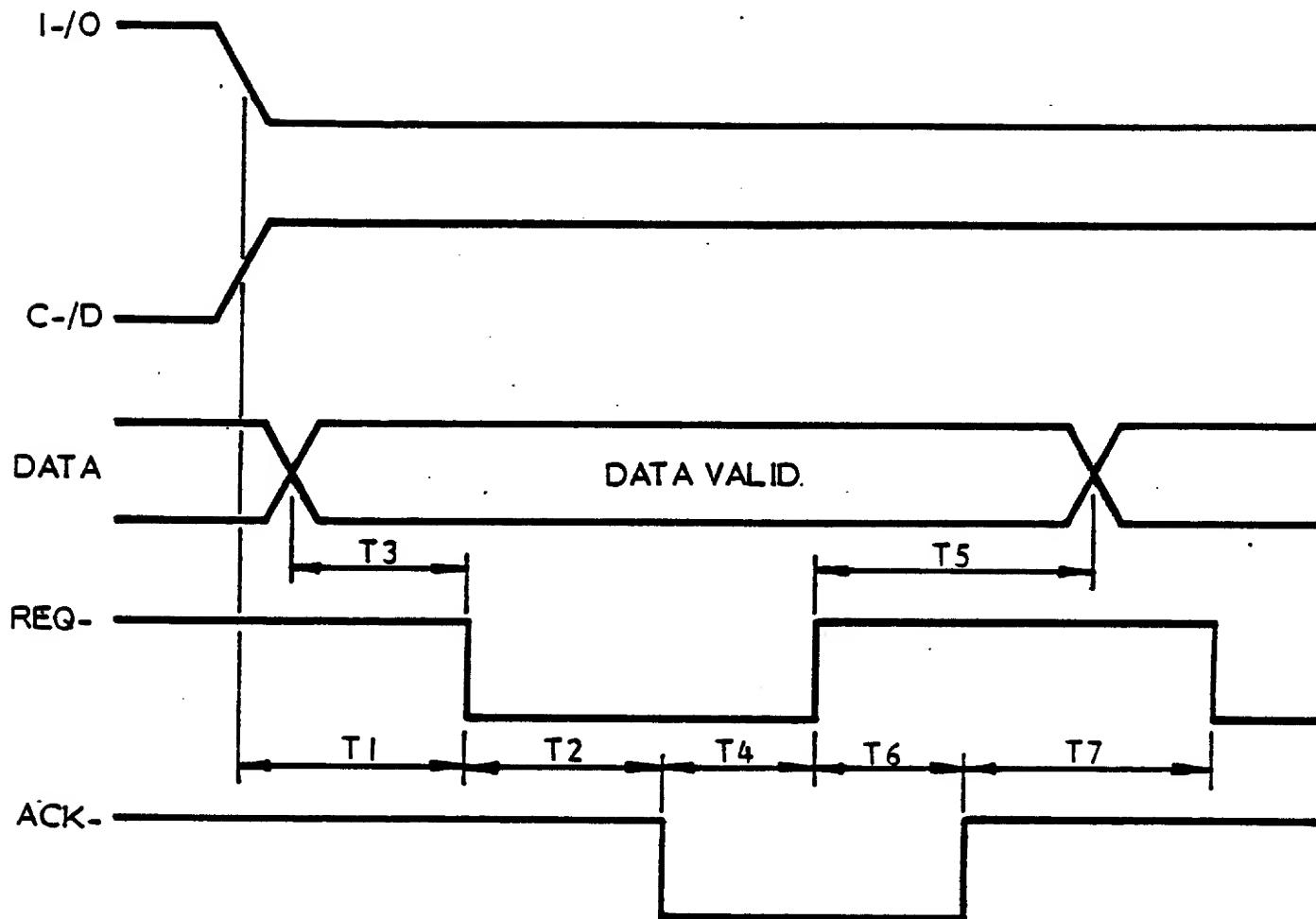
#### 4.3.2 Command Mode

The controller receives commands from the host adapter using a handshaking sequence. The controller places a low level on the C/D (command/data) line to indicate that it wants a command from the host adapter and places a high level on the I/O line to indicate that the movement of information is from the host adapter to the controller. The MSG- line is high.

The controller activates the REQ- line within 10 microseconds after signals I/O and C/D have been placed at high and low levels, respectively. The host adapter responds by activating the ACK- signal. The command byte placed on the data bus by the host must be stable within 250 nanoseconds after the ACK- signal is activated. The command byte must be held stable until REQ- is deactivated. The host deactivates ACK- after REQ- goes high. This completes the handshake for the first command byte. Each succeeding command byte from the host adapter requires the same complete handshake sequence.

#### 4.3.3 Data Transfer

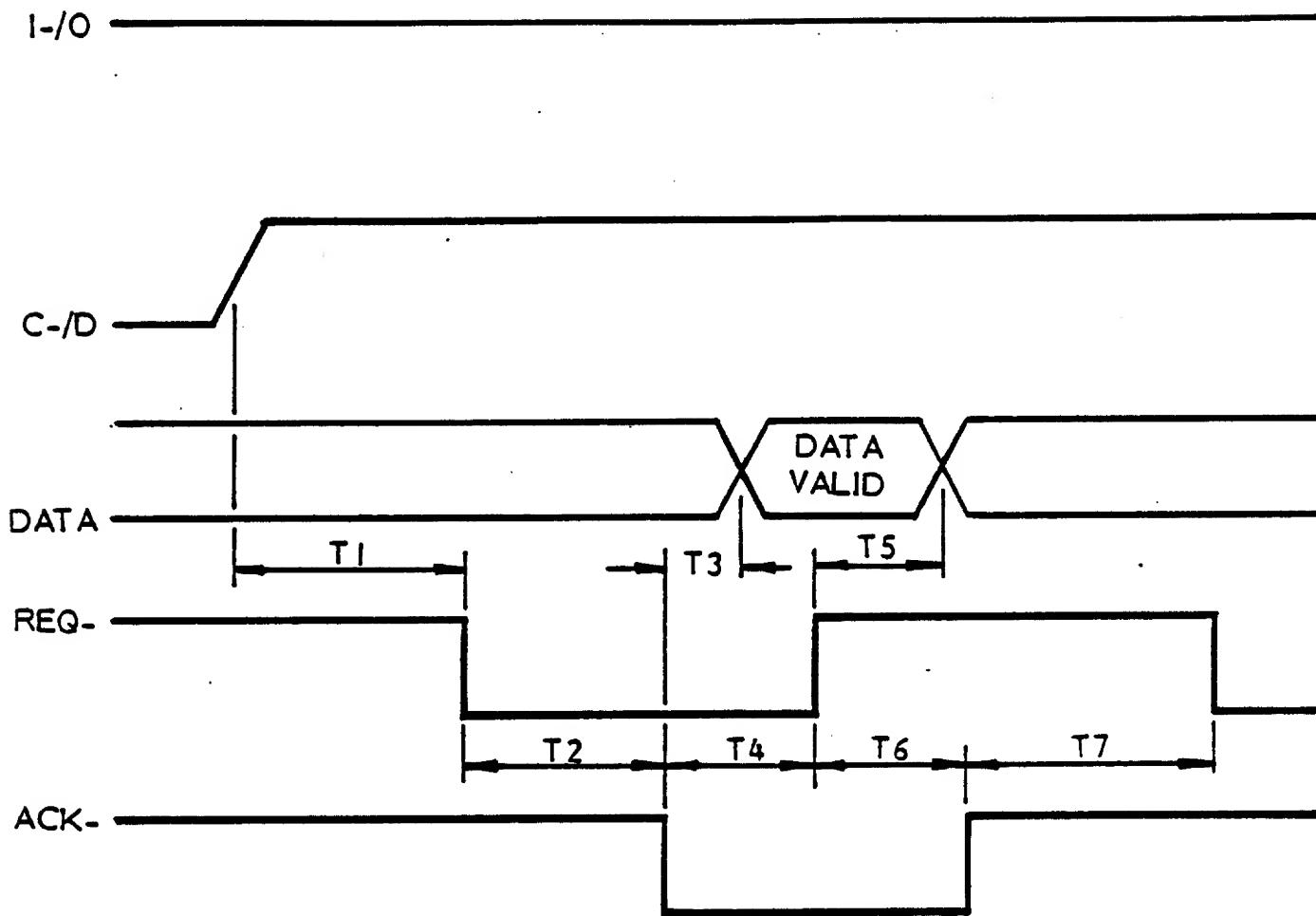
The timing diagrams in Figures 4-3 through 4-6 illustrate the required timing for data transfer.



**FIGURE 4-3 TIMING: DATA TRANSFER TO HOST FROM CONTROLLER**

- T1** = 10 microseconds (typ)
- T2** = no time limit
- T3** = 125 nanoseconds (min)
- T4** = 50 nanoseconds (typ)
- T5** = 100 nanoseconds (min)
- T6** = no time limit
- T7** = 10 nanoseconds (min)

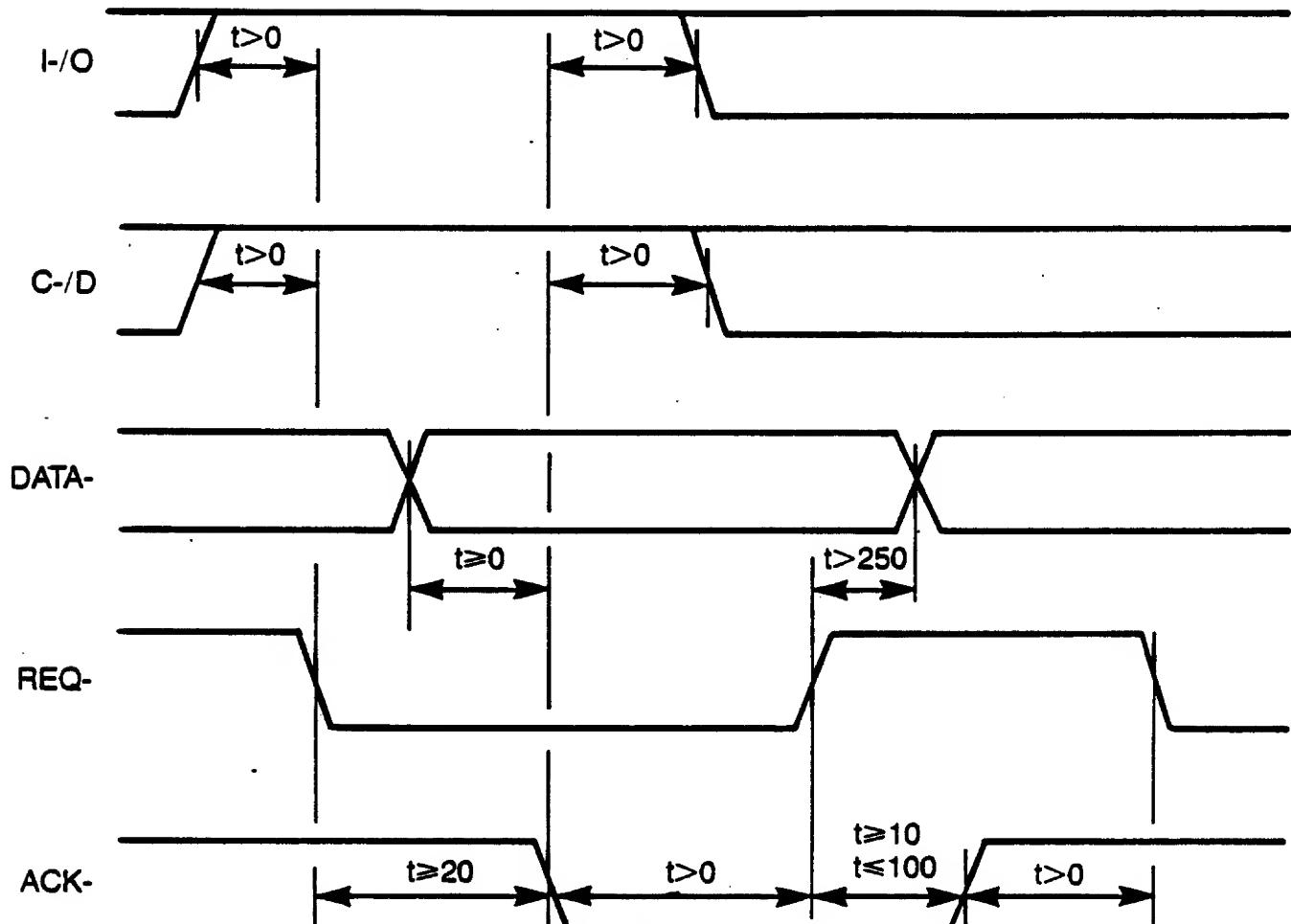
Maximum throughput rate is about 1 byte every 1.5 microseconds.



**FIGURE 4-4 TIMING: DATA TRANSFER FROM HOST TO CONTROLLER**

- T1** = 10 microseconds (typ)
- T2** = no time limit
- T3** = 250 nanoseconds (max)
- T4** = 750 nanoseconds (typ)
- T5** = 0 nanoseconds (min)
- T6** = no time limit
- T7** = 10 nanoseconds (min)

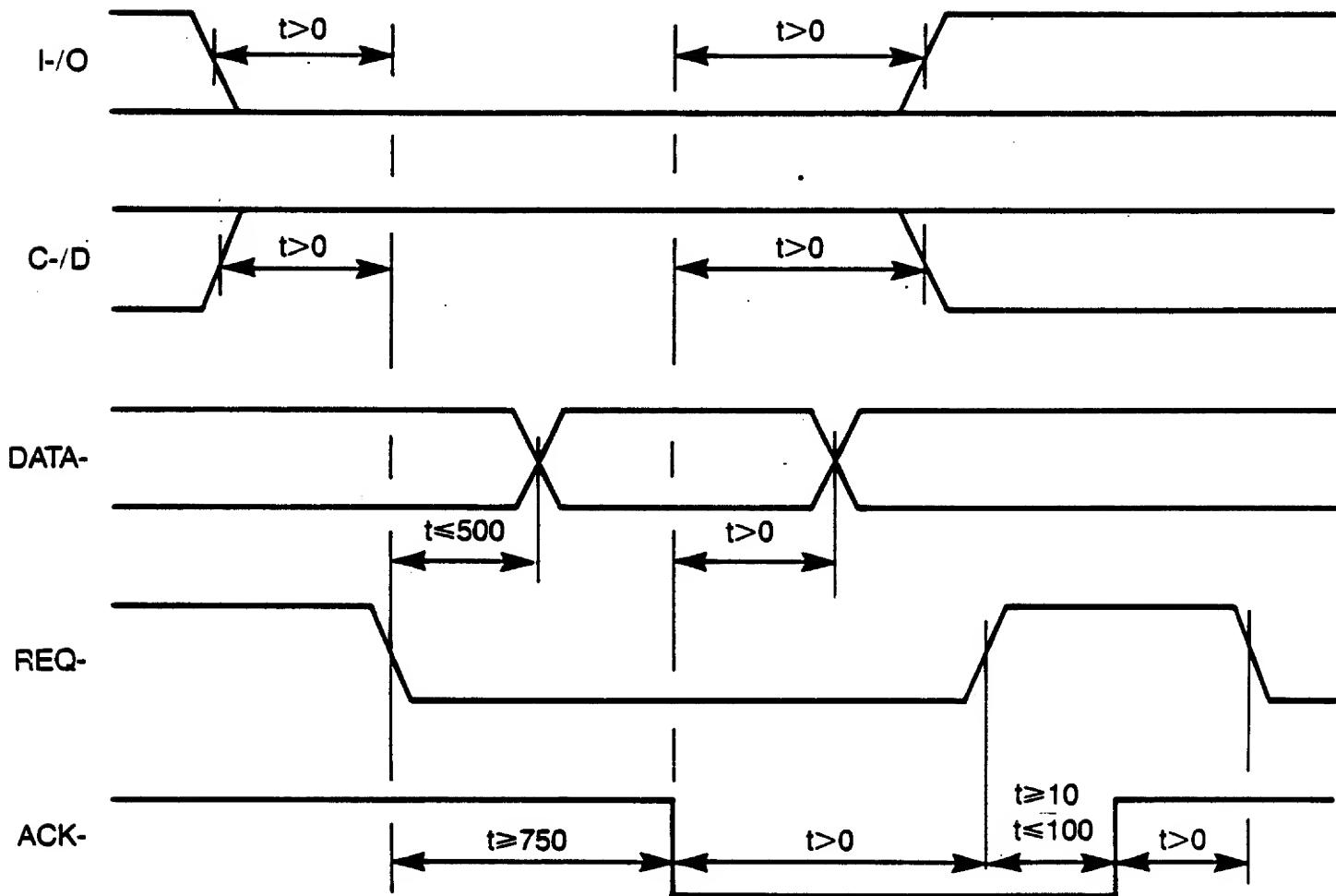
Maximum throughput rate is about 1 byte every 1.5 microseconds.



times are shown in nano-seconds

**FIGURE 4-5 DATA FROM THIS CONTROLLER TO ANOTHER CONTROLLER**

Maximum throughput approximately one byte every 1.25 microseconds.



times are shown in nano-seconds

**FIGURE 4-6 DATA TO THIS CONTROLLER FROM ANOTHER CONTROLLER**

Maximum throughput approximately one byte every microsecond.

#### 4.4 PROGRAMMING INFORMATION

The following paragraphs discuss communications between the controller and host from the point of view of the codes that are passed. The host sends commands to the controller through the host adapter. The controller then performs the commands and reports back to the host.

#### 4.5 COMMANDS

The host sends a six-byte block to the controller to specify the operation. This block is the Device Control Block (DCB). See Figure 4-7.

Bit	7	6	5	4	3	2	1	0
-----	---	---	---	---	---	---	---	---

Byte 0 Command Byte

Byte 1

Byte 2 - Sector Address

Byte 3

Byte 4 Interleave or Sector Count

Byte 5 Control Byte

**FIGURE 4-7 DEVICE CONTROL BLOCK (DCB), FORMAT**

**4.5.1 Byte 0:** The Command Byte. This is an 8-bit code to specify which of the defined commands is to be executed. Each command is described later in this section and summarized in the Appendix.

**4.5.2 Byte 4:** The interleave or Sector Count. For a format command, this byte is the interleave factor to use. The interleave factor must be less than the number of sectors per track. It may be 0 or 1, which will write consecutive sectors on the disk. For a read, write or copy command, this byte is the number of sectors to be transferred. A zero indicates 256 sectors are to be transferred.

- 4.5.3** **Byte 5:** The Control Byte. Each bit in this byte controls a particular feature.

Bit	7	6	5	4	3	2	1	0
R	P	0	0	0	0	0	0	0

- 4.5.3.1** Bit 7: Retry disable. If set, this will disable automatic retries for this command. If clear, the controller will attempt to execute this command up to 8 times before giving up and setting the error bit.
- 4.5.3.2** Bit 6: Bytes 1, 2 and 3 of the DCB specify a sector in the mass storage connected to this controller. The manner in which this sector is specified may be either using Physical Addressing or Logical Addressing. If this bit is one, Bytes 1, 2 and 3 will be decoded as a physical address. If this bit is zero, Bytes 1, 2 and 3 will be decoded as a logical address. See 4.5.4 and 4.5.5.
- 4.5.3.3** Bits 5-0: Reserved for later use.

#### 4.5.4 Physical Addressing.

If control byte bit 6 is set, specifying physical addressing, the specified sector is determined in the following way:

Bit	7	6	5	4	3	2	1	0
Byte 1	0	d	d	/	H	H	H	H
Byte 2	C	C	C	C	C	C	C	C
Byte 3	S	S	S	S	S	S	S	S

dd Selects one of four drives connected to the controller

HHHH Selects one of 15 heads or sides associated with the selected drive.  
Those heads are numbered 0 through E (hex).

CCCCCCCC Selects one of 255 cylinders associated with the selected drive. The cylinders are numbered 0 through FE (hex).

SSSSSSSS Selects one of 255 sectors on the specified cylinder, head and drive. These sectors are numbered 0 through FE (hex).

/ Don't care.

#### 4.5.5 Logical Addressing.

If control byte bit 6 is clear, specifying logical addressing, the specified sector is determined in the following way:

Bit	7	6	5	4	3	2	1	0
Byte 1	0	d	d	/	H	H	H	H
Byte 2	M	M	M	M	M	M	M	M
Byte 3	L	L	L	L	L	L	L	L

The logical address is a 20 bit address which is binary looks like:

HHHHMMMMMMMMMMLLL

H = high address, M = middle address, L = low address

- 4.5.6** Following are some equations to relate logical addressing to physical addressing.

Logical Address = (CYAD \* SDCYL + SDADR) \* SETRK + SEADR

**where:**

**CYADR** Cylindre Address (range 0 to FE)

**SDCYL**    Sides/Cylinder = # of heads (range 1 to F)

**SDADR** Side Address = Head Address (range 0 to E)

**SETRK** Number of sectors/track (range 1 to FF)

**SEADR** Sector Address (range 0 to FE)

**Track Number = CYADR \* SDCYL + SDADR**

**Physical Address may be written:**

Bit	7	6	5	4	3	2	1	0
Byte 1	0	LUN			SDADR			
Byte 2			CYADR					
Byte 3				SEADR				

where

LUN = logical unit number of drive, 0 to 3

#### **4.5.7 Test Drive Ready (Code 00)**

This command selects a particular drive and verifies that the drive is ready. The following diagram shows the format of the device control block of this command. 5%" drives will always return ready, since the drive does not return ready.

#### **4.5.8 Recalibrate (Code 01)**

This command positions the head(s) over track 00.

**d = drive, 0 to 3**

R = retries

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	0	1
Byte 1	0	d	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	R	0	0	0	0	0	0	0

#### 4.5.9 Request Sense Status (Code 03)

The host must send this command immediately after it detects an error. The command causes the controller to return four bytes of drive and Controller status; the formats of these four bytes are shown after the DCB. Table 4-6 lists the the error codes. Also, the errors are summarized in the appendix.

**d = drive, 0 to 3**

The 4 data bytes of status returned will look like

Bit	7	6	5	4	3	2	1	0
Byte 0	V	0						Error Code

If V is set, Bytes 1, 2 and 3 contain a Valid Address for the sector in which an error was found. An address is specified (physically or logically) in the same way as it was in the DCB. If V is clear, Bytes 1, 2 and 3 are undefined.

**TABLE 4-6 CONTROLLER ERROR CODES**

<u>HEX CODE</u>	<u>DEFINITION</u>
00	The controller detected no error during the execution of the previous operation.
02	The controller did not get a seek-complete signal.
04	After the controller selected the drive, the drive did not respond with ready signal.
06	After stepping maximum number of cylinders, controller did not receive track 00 signal from the drive.
07	The door on the floppy disk drive is open and needs to be closed to do the requested operation.
08	No head loaded.
10	An error was detected in the CRC of the target ID zone.
11	Write fault.
12	A write was attempted on a write protected floppy diskette.
14	Sector Not Found: The controller found the correct cylinder and head, but not the target sector.
15	Seek Error: The controller detected an incorrect cylinder or track, or both.
16	Format track timeout error.

**TABLE 4-6 CONTROLLER ERROR CODES (CONTINUED)**

<u>HEX CODE</u>	<u>DEFINITION</u>
17	Format track not complete.
19	Two sided error.
1A	Wrong data mark found.
1B	Pad Error: During a copy command the data transfer to/from the other controller did not agree with the sector transfer count provided in the command.
1D	Lost data in FDC.
1E	Data CRC error detected.
1F	FDC busy error. The LSI FDC chip was busy executing a command. This is a timeout or chip reset failure.
20	Invalid Command: The controller has received an invalid command from the host.
21	Illegal Disk Address. The controller detected an address that is not within the limits of the drive characteristics.
22	Something in the 8 bytes of data which specify the drive is not permissible.
23	Invalid interleave.
30	RAM Error: The controller detected a data error during the RAM sector-buffer diagnostic.
31	Program Memory Checksum Error: During its internal diagnostic, the controller detected a program-memory checksum error.

#### 4.5.10 Format Drive (Code 04)

This command formats all sectors with ID and data fields. Also, it writes E5 Hex or 40 Hex into data fields. E5 is for single density FM, 40 is for double density MFM. The starting address is passed in the DCB. The entire track on which that starting address is located and all subsequent tracks will be formatted. The sector size and density are specified by the Initialize Drive parameters command.

d = drive, 0 to 3

R = retries

P = Physical Addressing

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	0
Byte 1	0	0	d	/	High Address or Head Address			
Byte 2					Middle Address or Cylinder Address			
Byte 3					Low Address or Don't Care			
Byte 4					Interleave Factor			
Byte 5	R	P	0	0	0	0	0	0

#### 4.5.11 Format Track (Code 06)

This command formats a specified track. The command writes E5 Hex or 40 Hex into all data fields. E5 is for single density FM, 40 is for double density MFM. The track format is specified in the Initialize Drive Parameter command. The track which will be formatted is the track (cylinder address; head address and drive address) in which the specified sector is located. The specified sector need not be the first sector in the track.

d = drive, 0 to 3

R = retries

P = Physical Addressing

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	0
Byte 1	0	0	d	/	High Address or Head Address			
Byte 2	Middle Address or Cylinder Address							
Byte 3	Low Address or Don't Care							
Byte 4	Interleave Factor							
Byte 5	R	P	0	0	0	0	0	0

#### 4.5.12 Read (Code 08)

This command reads the specified number of sectors, starting with the initial sector address contained in the DCB. Each sector can be 128, 256, 512 or 1024 bytes of data. The sector size is determined at format time.

d = drive, 0 to 3

R = retries

P = Physical Address

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	0	0
Byte 1	0	d	d	/	High Address or Head Address			
Byte 2	Middle Address or Cylinder Address							
Byte 3	Low Address or Sector Address							
Byte 4	Sector Count							
Byte 5	R	P	0	0	0	0	0	0

#### 4.5.13 Write (Code 0A)

This command writes the specified number of sectors, starting with the initial sector address contained in the DCB. Each sector of data can be 128, 256, 512 or 1024 bytes long. The sector size is determined at format time.

**d = drive, 0 to 3**

**R = retries**

**P = Physical Address**

**D = Deleted Data Marks**

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	1	0
Byte 1	0	d	d	/	High Address or Head Address			
Byte 2	Middle Address or Cylinder Address							
Byte 3	Low Address or Sector Address							
Byte 4	Sector Count							
Byte 5	R	P	0	0	0	0	0	0

#### 4.5.14 Seek (Code 0B)

This command initiates a seek to the track specified in the DCB. The drive must be formatted.

**d = drive, 0 to 3**

**R = retries**

**P = Physical Address**

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	1	1
Byte 1	0	d	d	/	High Address or Head Address			
Byte 2	Middle Address or Cylinder Address							
Byte 3	Low Address or Don't Care							
Byte 4	/	/	/	/	/	/	/	/
Byte 5	R	P	0	0	0	0	0	0

#### 4.5.15 Initialize Drive Characteristics (Code 0C)

This command enables the user to configure the controller to work with drives that have different capacities and characteristics.

After the host sends the command (DCB) to the controller, it then sends an eight-byte block of data that contains the drive parameters. Some of the parameters occupy two bytes; all two-byte parameters are transferred with the most significant byte (MSB) first. The eight bytes are listed below.

Bit	7	6	5	4	3	2	1	0
-----	---	---	---	---	---	---	---	---

Byte 0	Number of Cylinders (range 1 to FF)							
Byte 1	0    0    r    r    4 Bit extension of Byte 2							
Byte 2	8" head Load or 5½" motor start timing in milliseconds							
Byte 3	4 bit code                          4 bit code (drive type: 8 or 5)                (number of heads: 1 to F)							
Byte 4	0    0    0    0    0    S    S    S							
Byte 5	Head unload time in tenths of seconds							
Byte 6	Number of sectors per track (range 1 to FF)							
Byte 7	f    f    0    0    0    0    0    0							

**4.5.15.1 Track switching rates.** "rr" is a 2 bit code to determine the track switching rates. See Table 4-7 below.

**TABLE 4-7 TRACK SWITCHING RATES**

<u>L</u>	<u>Drive Type</u>	<u>Stepping Time</u>
0 0	5½"	6 milli-seconds
0 1	5½"	12 milli-seconds
1 0	5½"	20 milli-seconds
1 1	5½"	30 milli-seconds
0 0	8"	3 milli-seconds
0 1	8"	6 milli-seconds
1 0	8"	10 milli-seconds
1 1	8"	15 milli-seconds

**4.5.15.2** To clarify Byte 3, the left most 4 bits must contain an 8 or a 5 (right justified). The right most 4 bits contain the number of heads on the drive. For example:

52 (hex) = 5½" with 2 heads

81 (hex) = 8" drive with 1 head

**4.5.15.3** Byte 4 contains the data field size of a sector on the drive. The sizes are listed in Table 4-8.

**TABLE 4-8 SECTOR SIZE**

<u>S</u>	<u>S</u>	<u>S</u>	<u>SECTOR SIZE</u>
0	0	0	128 bytes
0	0	1	256 bytes
0	1	0	512 bytes
1	0	0	1024 bytes

**4.5.15.4** Byte 5 sets the timeout between completion of a command and unloading the head from the media. The time is specified in tenths of seconds.

**4.5.15.5** Byte 7 dictates the recording density used. There are currently three defined types.

**00 (hex):** Recording format is FM, single density. If 128 bytes/sector and 26 sectors/trade, 8" drive, this is IBM's 3740 single density format.

**40 (hex):** Recording density is MFM, double density, on all tracks except track 00 where it is FM. On track 00 only, the number of bytes per sector will be one half of what is specified in Bytes 4 and 5. If the disk is formatted in 256 bytes/sector and 26 sectors/trade and 8" drive, this is IBM's System-34 double density format.

**C0 (hex):** Recording density is MFM, double density, all tracks.

See Table 4-9 for the physical constraints of what combinations of drive initialize characteristics are allowed.

TABLE 4-9 TRACK CAPACITY

	<u>BYTES/SECTOR</u>	<u>8"</u>	<u>5½"</u>	<u>FORMAT</u>
00 (hex)	128	26	16	FM*
	256	15	9	FM
	512	8	5	FM
	1024	4	2	FM
40 (hex)	256	26	16	MFM**
	512	15	9	MFM
	1024	8	5	MFM
(In the 3 above cases, track 0 will have $\frac{1}{2}$ as many bytes/sector, and be recorded in FM.)				
C0 (hex)	128	40	24	MFM
	256	26	16	MFM
	512	15	9	MFM
	1024	8	5	MFM

\*IBM's 3740 Format

\*\*IBM's System - 34 Format

**4.5.15.6 Default Drive.** If no drive initialization is specified, the drive characteristics will default to the following parameters.

Number of cylinders = 35

Number of heads = 1

Sector size = 256

Drive type = 5

Motor Start Timing = 1 second

Track Stepping Rate = 30 milli-seconds

**4.5.16 Copy From Floppy Disk Command (Code C1)**

This command reads the specified numbers of sectors, starting with the initial sector address contained in the DCB. The command is designed to transfer data directly to another intelligent controller, such as the S1410 or another S1401, on the same SASI bus.

Software must issue the command DCB to the Floppy Disk Controller, request status, and then issue the Write Command to the other controller. As soon as the other controller goes from command to data transfer mode, the FDC will send data to the other controller. Data transfer will stop when the other controller goes back into command mode to terminate the data transfer and return status to the host. If the data transfer does not end when the sector count in the FDC goes to zero, the FDC will return an error. If the FDC encounters an error during operation, the FDC will pad data to the other controller to prevent a bus hang. The other controller must move data in some multiple of 128 byte blocks.

d = drive, 0 to 3

R = retries

P = Physical Address

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	0	0	0	0	0	1
Byte 1	0	d	d	/	High Address or Head Address			
Byte 2					Middle Address or Cylinder Address			
Byte 3					Low Address or Sector Address			
Byte 4					Sector Count			
Byte 5	R	P	0	0	0	0	0	0

#### 4.5.17

#### Copy to Floppy Disk Command (Code C2)

This command writes the specified number of sectors, starting with the initial sector address contained in the DCB. This command is designed to transfer data directly from another intelligent controller, such as the S1410 or the S1410, on the same SASI bus.

Software must issue this command DCB to the Floppy Disk Controller, request status, and then issue the read command to the other controller. As the other controller goes from command to data transfer mode, the FDC will receive data from the other controller. Data transfer will stop when the other controller goes back into command mode to terminate the data transfer and return status to the host. If the data transfer does not end when the sector count in the FDC goes to zero, the FDC will return an error. If the FDC encounters an error during operation, the FDC will continue to accept data until the other controller completes the data transfer to prevent a bus hang. The other controller must move data in some multiple of 128 byte blocks.

d = drive, 0 to 3

R = retries

P = Physical Address

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	0	0	0	0	1	0
Byte 1	0	d	d	/	High Address or Head Address			
Byte 2					Middle Address or Cylinder Address			
Byte 3					Low Address or Sector Address			
Byte 4					Sector Count			
Byte 5	R	P	0	0	0	0	0	0

#### 4.5.18 RAM Diagnostic (Code E0)

This command performs a data pattern test on the RAM buffer.

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	0	0	0
1	/	/	/	/	/	/	/	/
2	/	/	/	/	/	/	/	/
3	/	/	/	/	/	/	/	/
4	/	/	/	/	/	/	/	/
5	/	/	/	/	/	/	/	/

#### 4.5.19 Drive Diagnostic (Code E3)

This command tests both the drive and the drive-to-controller interface. The controller sends recalibrate and seek commands to the selected drive and verifies sector 0 of all the ID fields on the disk. The controller does not perform any write operations during this command; it is assumed that the disk has been previously formatted.

**d = drive, 0 to 3**

R = retries

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	0	1	1
Byte 1	0	d	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	R	0	0	0	0	0	0	0

#### **4.5.20 Controller Internal Diagnostics (Code E4)**

This command causes the controller to perform a self-test. The controller checks its internal processor, data buffers, and the checksum of the program memory. The controller does not access the disk drive.

#### 4.5.21 COMMAND COMPLETION

When the Floppy Disk Controller has completed execution of its command, which may or may not include a data transfer, it will send two final bytes of status over the SASI bus. They will look like this:

##### NEXT TO LAST BYTE

Bit	7	6	5	4	3	2	1	0
	0	d	d	0	0	0	E	0

dd            drive specified in DCB (range 0 to 3)

E            error flagged if set

##### LAST STATUS BYTE

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0

After which the controller will clear busy and wait to be selected again. If the command was a copy command, this does not apply because the Floppy Disk Controller will clear BUSY- shortly after receiving the command and no final status bytes will be sent.

#### 4.6 SECTOR FORMAT

Tables 4-10 and 4-11 show the formats of the sector and the names of the fields of the information traveling over the Controller-drive interface.

TABLE 4-10 FDD SECTOR/TRACK FORMAT FM

<u>DATA</u>	<u># OF BYTES</u>	
FF	40	Post Index Gap, beginning at Index hole
00	6	Sync Field
FC	1	Index Address Mark
FF	26	Gap
00	6	Sync Field
FE	1	I.D. Address Mark
XX	1	Track Number (range 0 to FE)
0X	1	Head Number (range 0 to E)
Repeated	XX	Sector Number (range 0 to FE)
Once for Each	0X	Sector Length (X = 0, 1, 2, 3: Sector length = 128, 256, 512, 1024)
Sector	XX	CRC
FF	11	Gap
00	6	Sync Field
FB	1	Data Address Mark
E5	?	Data Field (# Bytes = 128, 256, 512 or 1024)
XX	2	CRC
FF	27	Gap
FF	?	Pre-Index Gap written from end of last sector to the index hole

The data fields are formatted with E5 (Hex) as the data.

TABLE 4-11 FDD SECTOR/TRACK FORMAT, MFM

<u>DATA</u>	<u># OF BYTES</u>	
4E	80	Post Index Gap, beginning at Index hole
00	12	Sync Field
C2	3	
FC	1	Index Address
4E	50	Gap
00	12	Sync Field
A1	3	
FE	1	I.D. Address Mark
XX	1	Track Number (range 0 to FE)
0X	1	Head Number (range 0 to E)
Repeated	XX	Sector Length (X = 0, 1, 2, 3: Sector length = 128, 256, 512, 1024)
Once for		
Each	XX	CRC
Sector	4E	Gap
00	12	Sync Field
A1	3	
FB	1	Data Address Mark
40	?	Data Field (# bytes = 128, 256, 512, 1024)
XX	2	CRC
4E	54	Gap
4E	?	Pre index gap. Written from end of last sector to index hole.

The data fields are formatted with 40 (Hex) as the data.

## APPENDIX

### CONTENTS.

- 5.1 Error Codes
- 5.2 Error Code Summary
- 5.3 Command Code Summary
- 5.4 Further Explanations and Clarifications
  - 5.4.1 Execution of Diagnostics
- 5.5 Drive Characteristics

## APPENDIX

### 5.1 ERROR CODES.

When a Request Sense Status command is sent to the controller, the first byte sent back is the error code byte and is defined as follows:

Bits 0-5	Error code
Bit 6	Spare, set to zero
Bit 7	Address valid when set

The address valid bit in the error code byte (bit 7) is relevant only when the previous command required a sector address in which case it is always returned as a one otherwise it is set to zero. For instance, if a Recalibrate command were followed immediately by a Request Sense Status command, the address valid bit would be returned as zero since this command does not require a logical block address to be passed in its DCB.

## APPENDIX

**5.3 ERROR CODE SUMMARY.**

The following is a summary of the error codes returned as the result of the Request Sense Status command.

NOTE: The address valid bit (bit 7) may or may not be set and is not included here for clarity.

<u>Error Code (hex)</u>	<u>Meaning.</u>
00 .....	No error detected (command completed ok).
02 .....	Seek timeout.
04 .....	Drive not ready after it was selected.
06 .....	Track 00 not found.
07 .....	Door open.
08 .....	No head loaded.
10 .....	ID CRC error.
11 .....	Write fault.
12 .....	Read-only error.
14 .....	Sector not found.
15 .....	Seek error.
16 .....	Format track timeout error.
17 .....	Format track not complete.
19 .....	Two side error (diskette wrong).
1A .....	Wrong data mark.
1B .....	Transfer length error.
1D .....	Lost data in FDC.
1E .....	Data CRC error.
1F .....	FDC busy error.
20 .....	Invalid command received.
21 .....	Illegal disk address.
22 .....	Invalid drive initialize data.
23 .....	Invalid interleave.
30 .....	Ram diagnostic failure.
31 .....	Program memory checksum error.

**APPENDIX****5.4 COMMAND CODE SUMMARY.**

<u>Command Code (hex)</u>	<u>Page</u>	<u>Meaning</u>
00 .....	35 .....	Test drive ready.
01 .....	36 .....	Recalibrate (position heads on tract).
03 .....	36 .....	Request sense status.
04 .....	40 .....	Format disk drive.
06 .....	40 .....	Format track.
08 .....	41 .....	Read.
0A .....	41 .....	Write.
0B .....	42 .....	Seek.
0C .....	43 .....	Initialize drive characteristics.
C1 .....	47 .....	Copy from floppy disk.
C2 .....	48 .....	Copy to floppy.
E0 .....	49 .....	Ram diagnostic.
E3 .....	49 .....	Drive diagnostic.
E4 .....	50 .....	Controller internal diagnostics.

## APPENDIX

### 5.4 FURTHER EXPLANATIONS AND CLARIFICATIONS.

#### 5.4.1 Execution of Diagnostics.

Since all of the diagnostics are not executed by the controller on power up, it is suggested that they be envoked by the host in the following order:

- 1) Controller internal diagnostics (Command Code E4). This diagnostic tests all the logical and decision making capability of the controller as well as the program memory checksum. Execution of this diagnostic first ensures that the controller can communicate with the host.
- 2) The Ram Diagnostic (Command Code E0) should be executed next. This command verifies that the sector buffer is operational by writing, reading and verifying various data patterns to and from all locations.
- 3) If the parameters of the connected drives are different than the default parameters listed on page 45, the new configuration must be sent to the controller using the Initialize Drive Characteristics command (Command Code 0C) before the Drive Diagnostic is executed. (See Appendix Section 5.7 for the configuration parameters of various disk drives).
- 4) Before the Drive Diagnostic is executed, the host program should continuously issue a Test Drive Ready command to the controller (Command Code 00) with the appropriate time-out until the drive becomes ready.
- 5) Drive Diagnostic (Command Code E3). This diagnostic issues a Recalibrate to the disk drive and then steps through all tracks verifying the CRC on the identifier fields of the first sector of each track. If this diagnostic passes, it implies that the disk has been formatted and that the first ID field of each track is good.